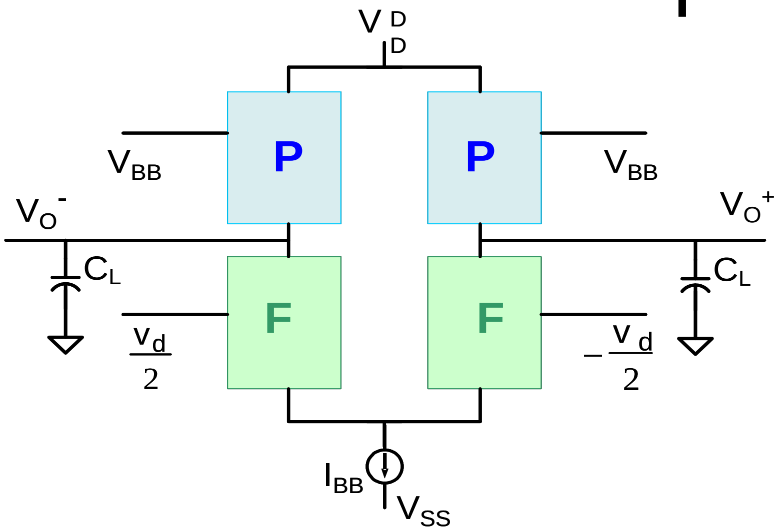
EE 435

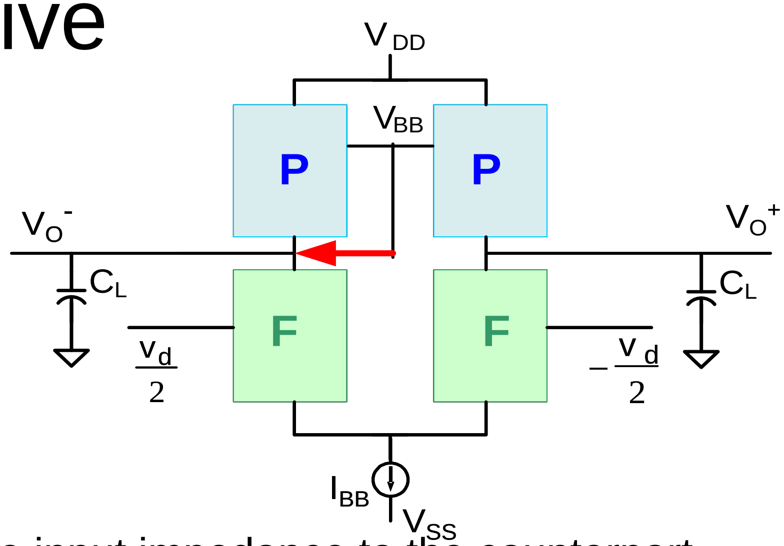
Lecture 6:

- Signal Swing
- Measurement/Simulation of High Gain Circuits
- Offset Voltage
- High Gain Single-Stage Op Amps

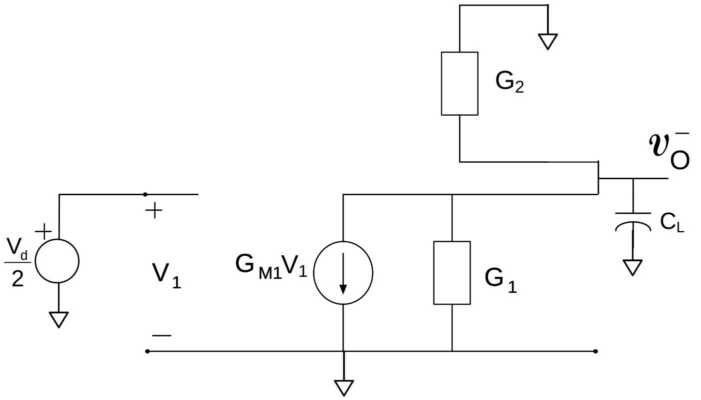
Review from last lecture:

Operation of Op Amp – A different perspective





Small signal differential half-circuit



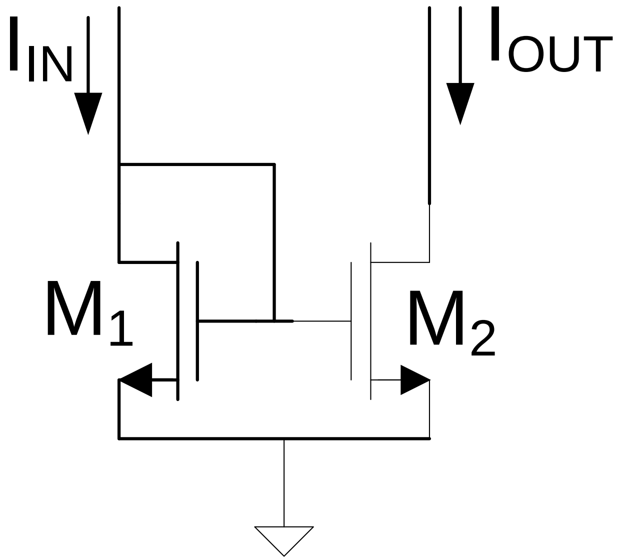
If the input impedance to the counterpart circuit is infinite and the quiescent values of the left and right drain voltages are the same, connecting the bias port of the quarter circuit to V_0^- instead of to V_{BB} will cause the signal current in the right counterpart circuit to be equal to that in the left counterpart circuit

This will double the signal current steered to V_o^+ and thus double the voltage gain !

This will also eliminate the need for a CMFB circuit !

Review from last lecture:

Basic Current Mirror



n-channel

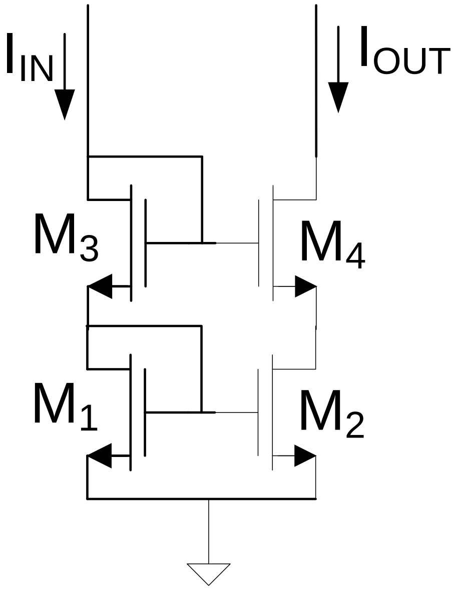
$$I_{IN} = \frac{\mu C_{OX} W_1}{2L_1}\left(V_{GS1}\text{-}V_T\right)^2$$

$$I_{OUT} = \frac{\mu C_{OX} W_2}{2L_2}\left(V_{GS2}\text{-}V_T\right)^2$$

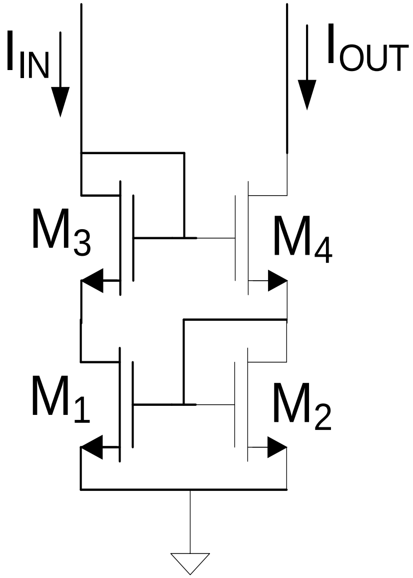
$$\frac{I_{OUT}}{I_{IN}} = \frac{W_2}{W_1}\frac{L_1}{L_2}$$

Review from last lecture:

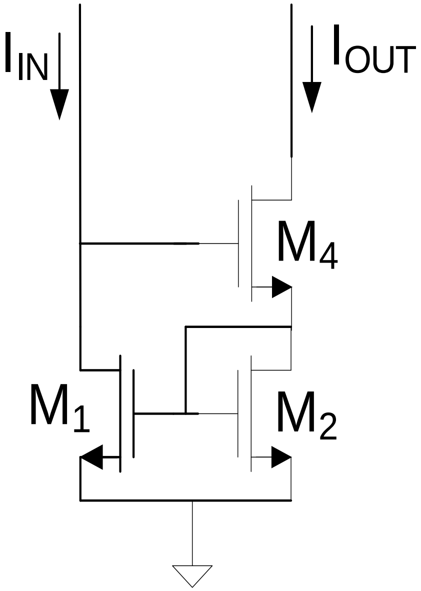
More Advanced Current Mirrors



Cascode Current
Mirror



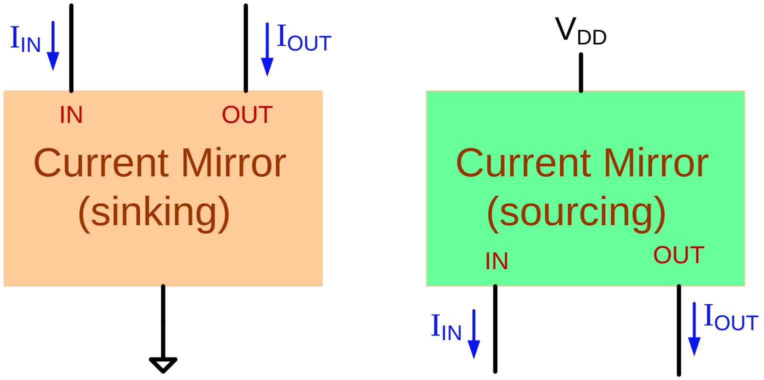
Modified Wilson
Current Mirror



Wilson Current
Mirror

Review from last lecture:

USPTO search on Feb 2, 2021



605 patents with “current and mirror” in title since 1976

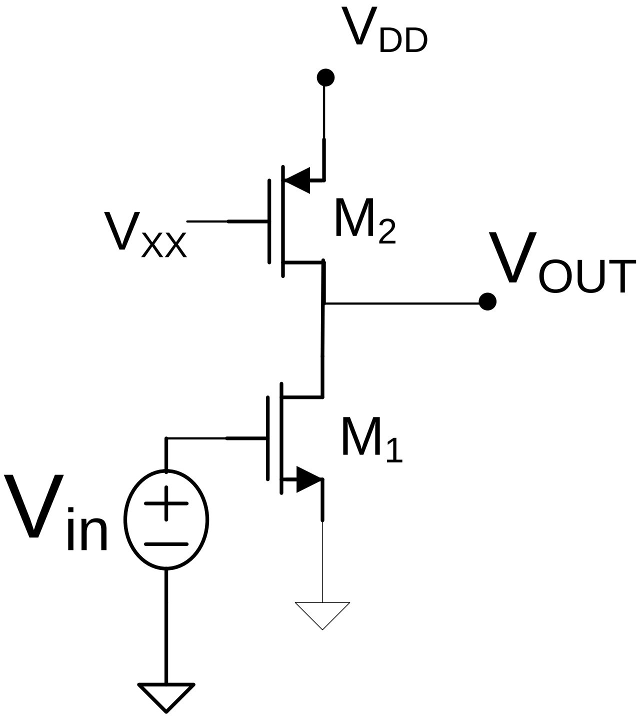
26 patents with “current and mirror” in title from 2018 and 2020 searches

Number of patents/year is about at the 3-decade average

Is there still an opportunity to contribute to the current mirror field?

Review from last lecture:

Signal Swing



To keep M_1 out of Triode Region

$\mathcal{L}_1$: $V_{OUT} > V_{iN} - V_{Tn}$

To keep M_1 out of Cutoff

$\mathcal{L}_2$: $V_{iN} > V_{Tn}$

To keep M_2 out of Triode Region

$\mathcal{L}_3$: $|V_{OUT} - V_{DD}| > |V_{XX} - V_{DD} - V_{Tp}|$

$$\Rightarrow V_{XX} - V_{Tp} > V_{OUT}$$

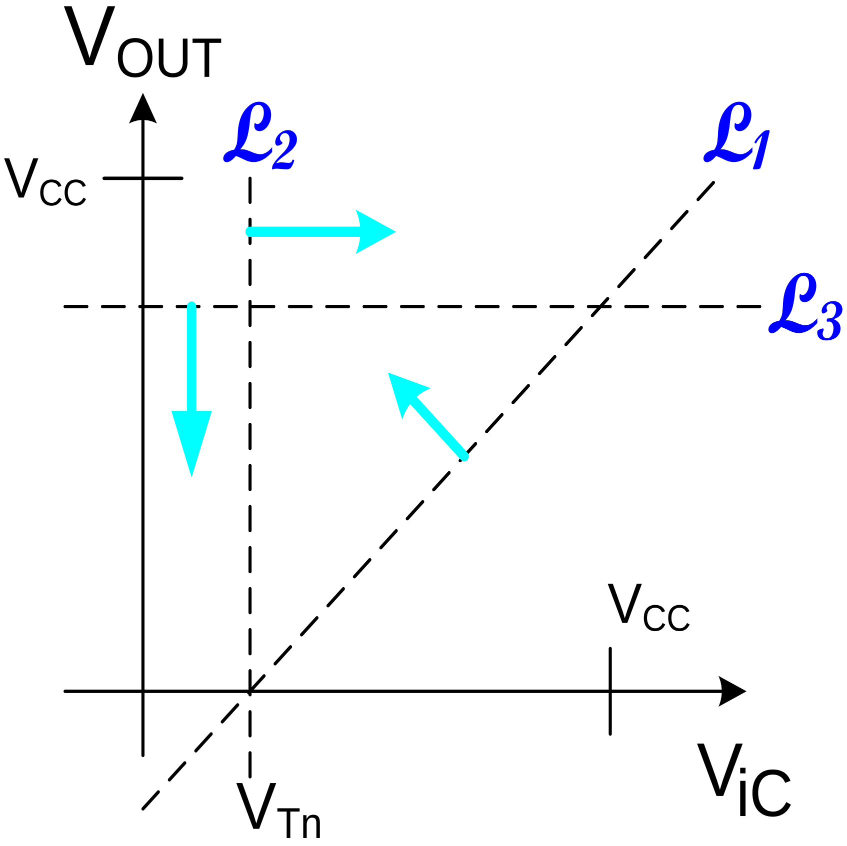
Review from last lecture:

Signal Swing

$\mathcal{L}_1$: $V_{OUT} > V_{iN} - V_{Tn}$

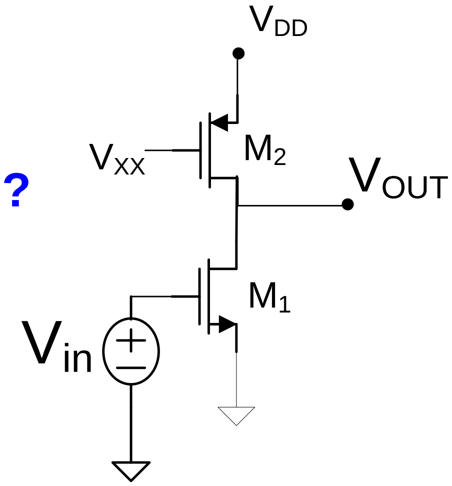
$\mathcal{L}_2$: $V_{iN} > V_{Tn}$

$\mathcal{L}_3$: $V_{XX} - V_{Tp} > V_{OUT}$

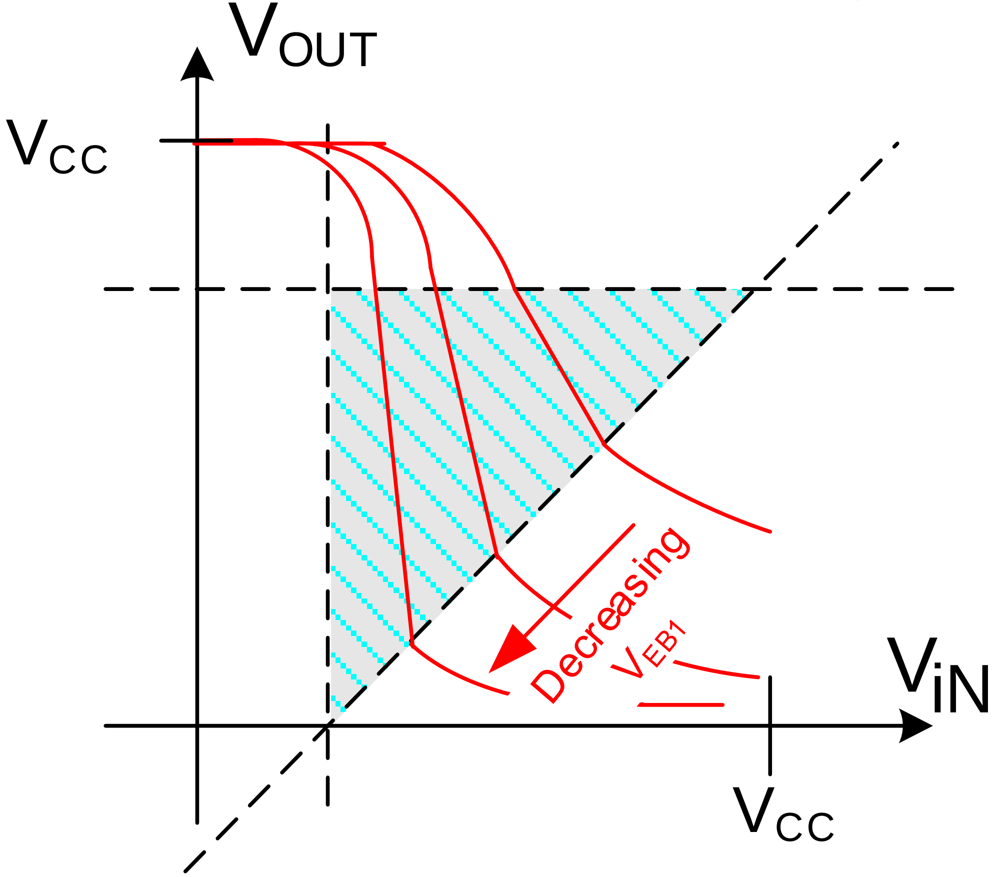


Review from last lecture:

Signal Swing

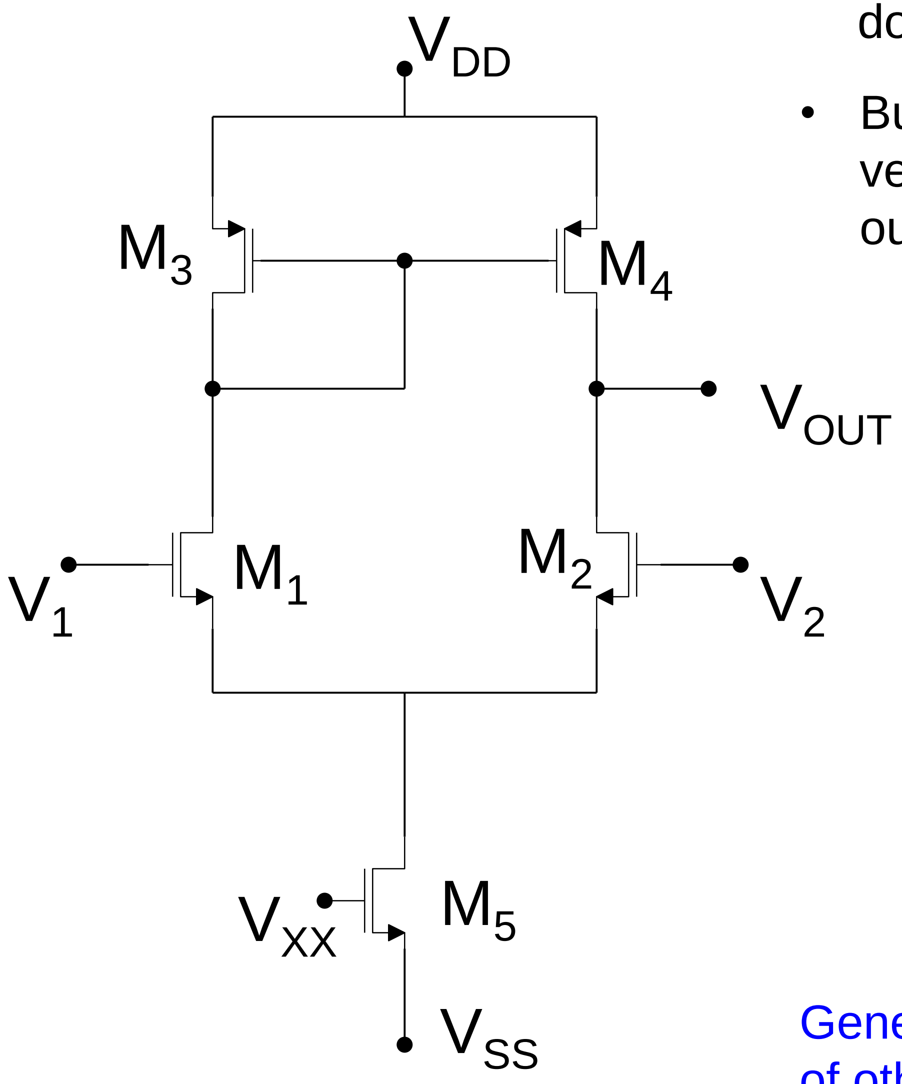


How do the transfer characteristics relate to the signal swing ?

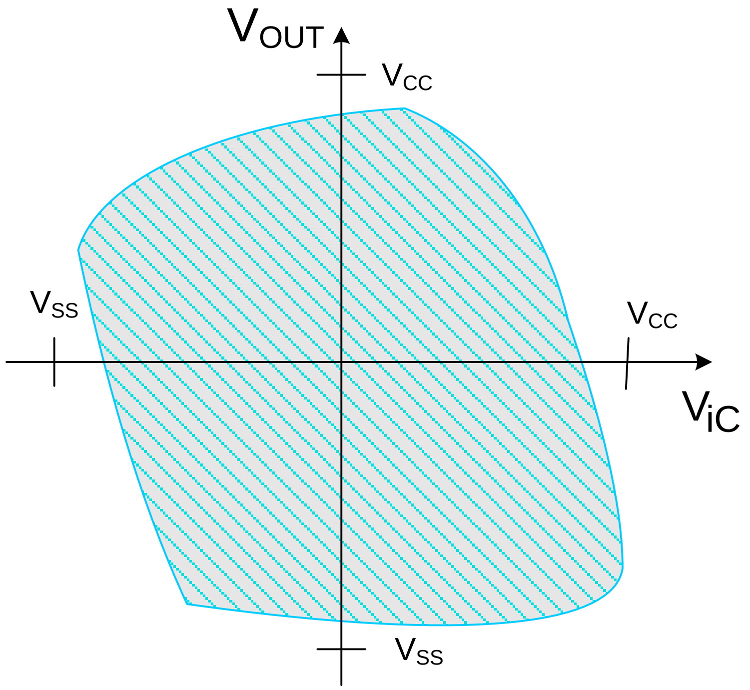


For this circuit, high gain and large output signal swing for small V_{EB1}

Signal Swing of Single-Stage Op Amp



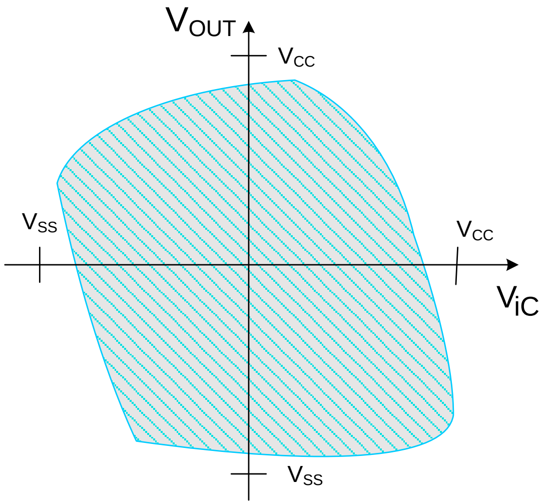
- Interested in region in {V_{iC}, V_d, V_{OUT}} domain where op amp operates
- But for high-gain amplifiers, V_d is inherently very small so are only concerned about output signal swing vs V_{iC}



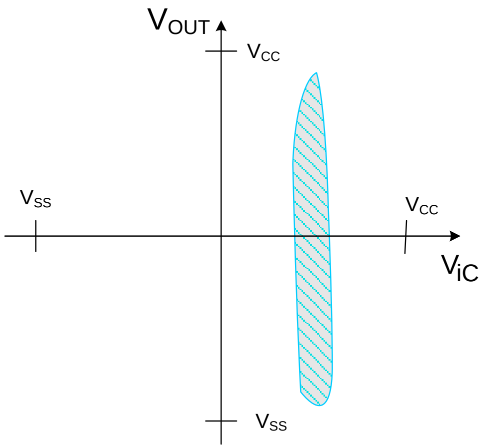
Generally large swings come at expense of other desirable characteristics

Signal Swing of Single-Stage Op Amp

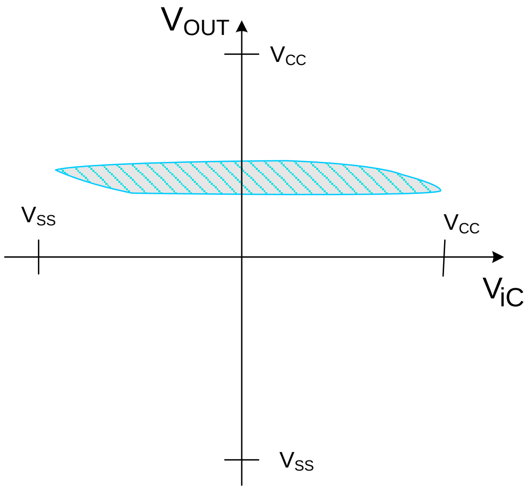
What type of signal swing is needed ?



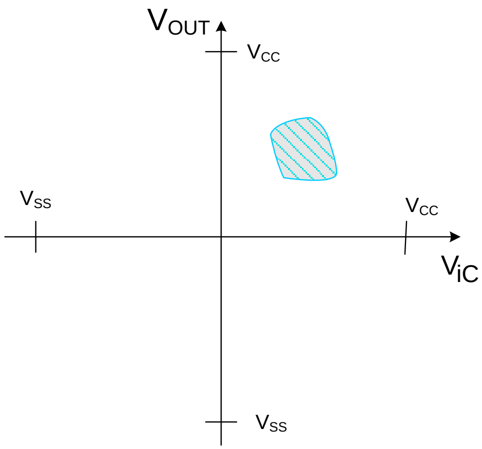
Wide V_{iC} and V_{OUT} range



Narrow V_{iC} and wide V_{OUT} range



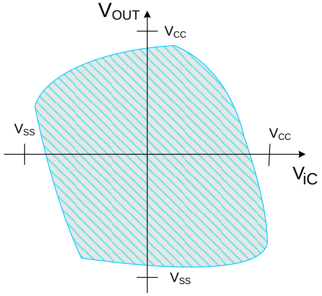
Narrow V_{OUT} and wide V_{iC} range



Narrow V_{iC} and V_{OUT} range

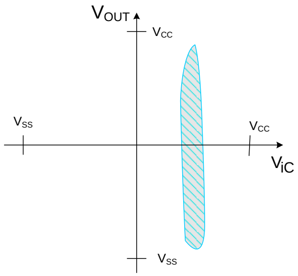
Signal Swing of Single-Stage Op Amp

What type of signal swing is needed ?



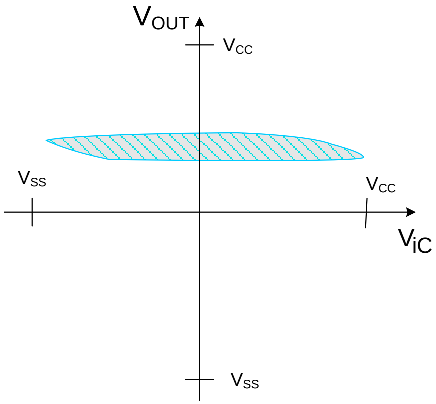
Wide V_{iC} and V_{OUT} range

Expected for catalog parts and overall I/O in many applications



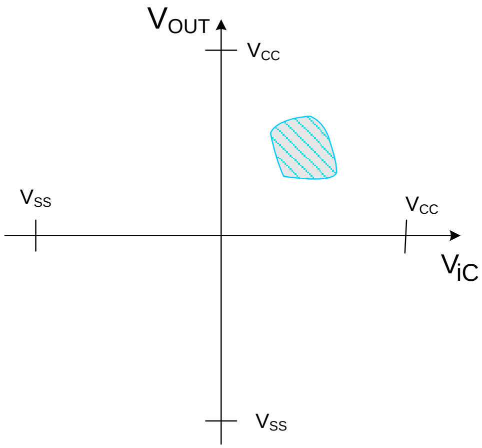
Narrow V_{iC} and wide V_{OUT} range

Acceptable when ViC is fixed



Narrow V_{OUT} and wide V_{iC} range

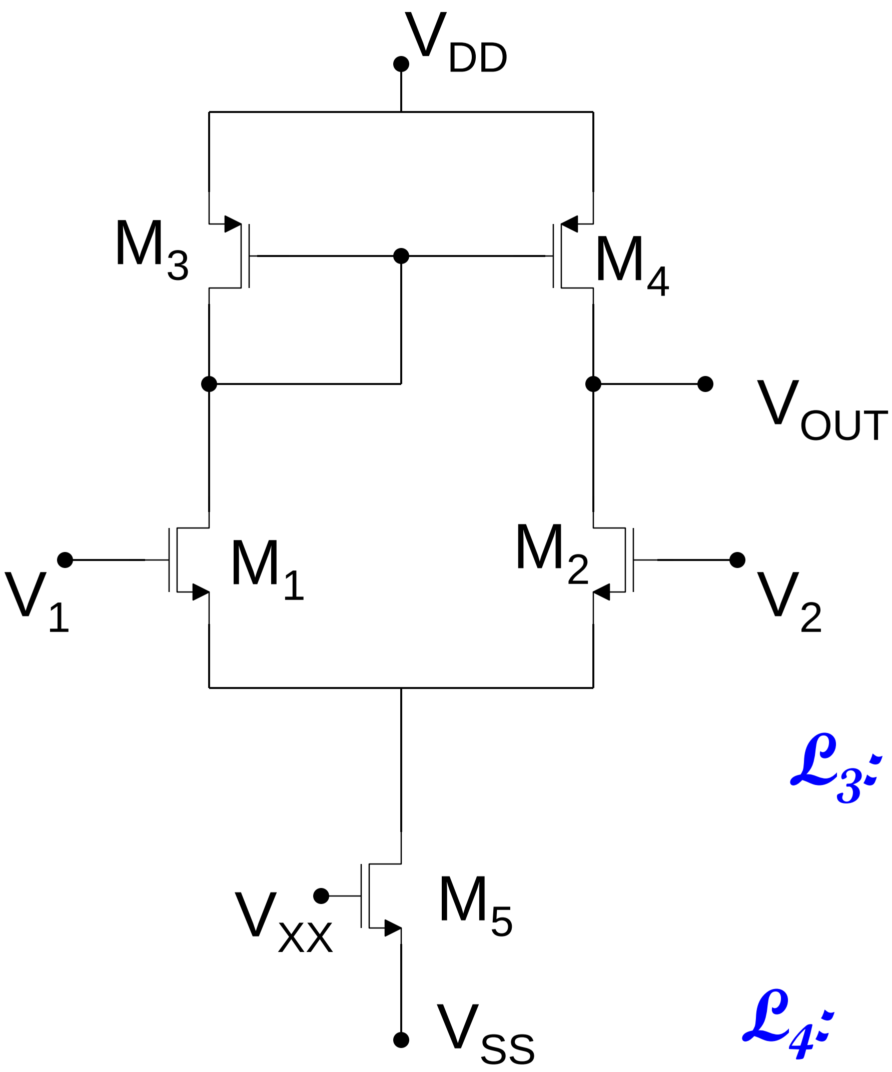
Acceptable when followed by high-gain stage



Narrow V_{iC} and V_{OUT} range

Acceptable when V_{iC} fixed and followed by high-gain stage

Signal Swing of Single-Stage 5T Op Amp



Constraining Equations:

To keep M_2 in Saturation:

$\mathcal{L}_1$: $$V_{OUT} > V_{ic} - V_{T2}$$

To keep M_4 in Saturation:

$\mathcal{L}_2$: $$V_{OUT} < V_{DD} - \left|V_{EB4}\right|$$

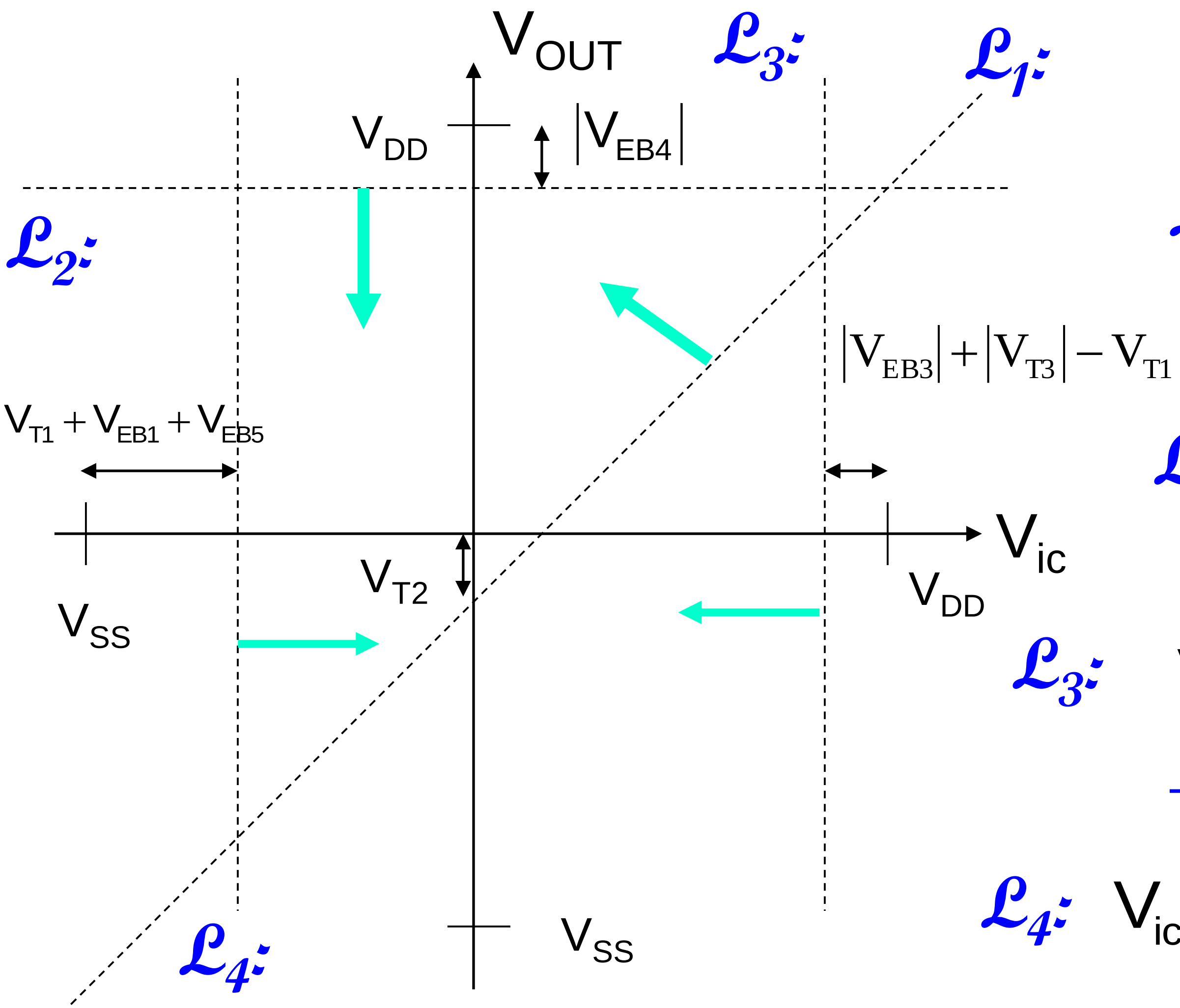
To keep M_1 in Saturation:

$\mathcal{L}_3$: $$V_{iC} < V_{DD} + V_{T1} - \left|V_{T3}\right| - \left|V_{EB3}\right|$$

To keep M_5 in Saturation:

$\mathcal{L}_4$: $$V_{ic} > V_{T1} + V_{EB1} + V_{EB5} + V_{SS}$$

Signal Swing of Single-Stage 5T Op Amp



To keep M_2 in Saturation:

$\mathcal{L}_1$: $V_{OUT} > V_{ic} - V_{T2}$

To keep M_4 in Saturation:

$\mathcal{L}_2$: $V_{OUT} < V_{DD} - |V_{EB4}|$

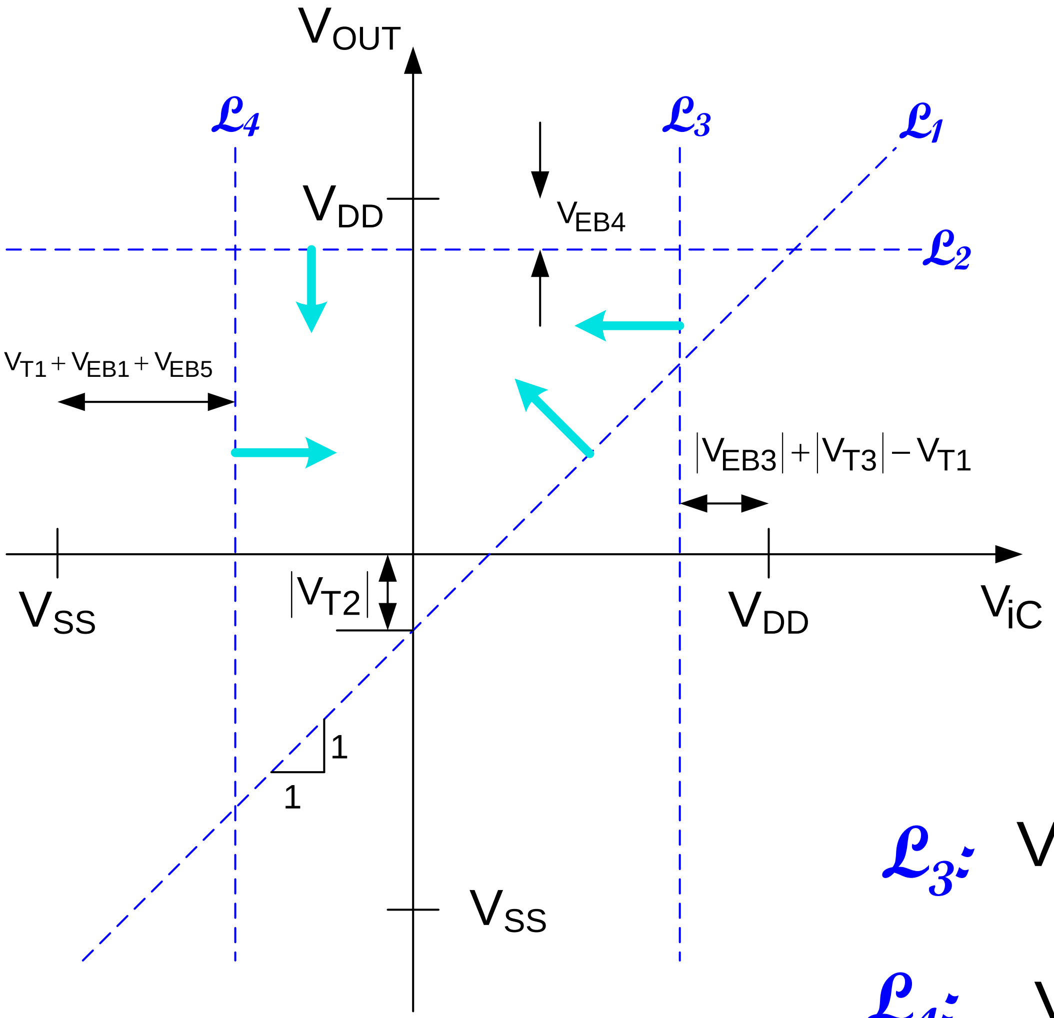
To keep M_1 in Saturation:

$\mathcal{L}_3$: $V_{iC} < V_{DD} + V_{T1} - |V_{T3}| - |V_{EB3}$

To keep M_5 in Saturation:

$\mathcal{L}_4$: $V_{ic} > V_{T1} + V_{EB1} + V_{EB5} + V_{SS}$

Signal Swing of Single-Stage 5T Op Amp



Constraining Equations:

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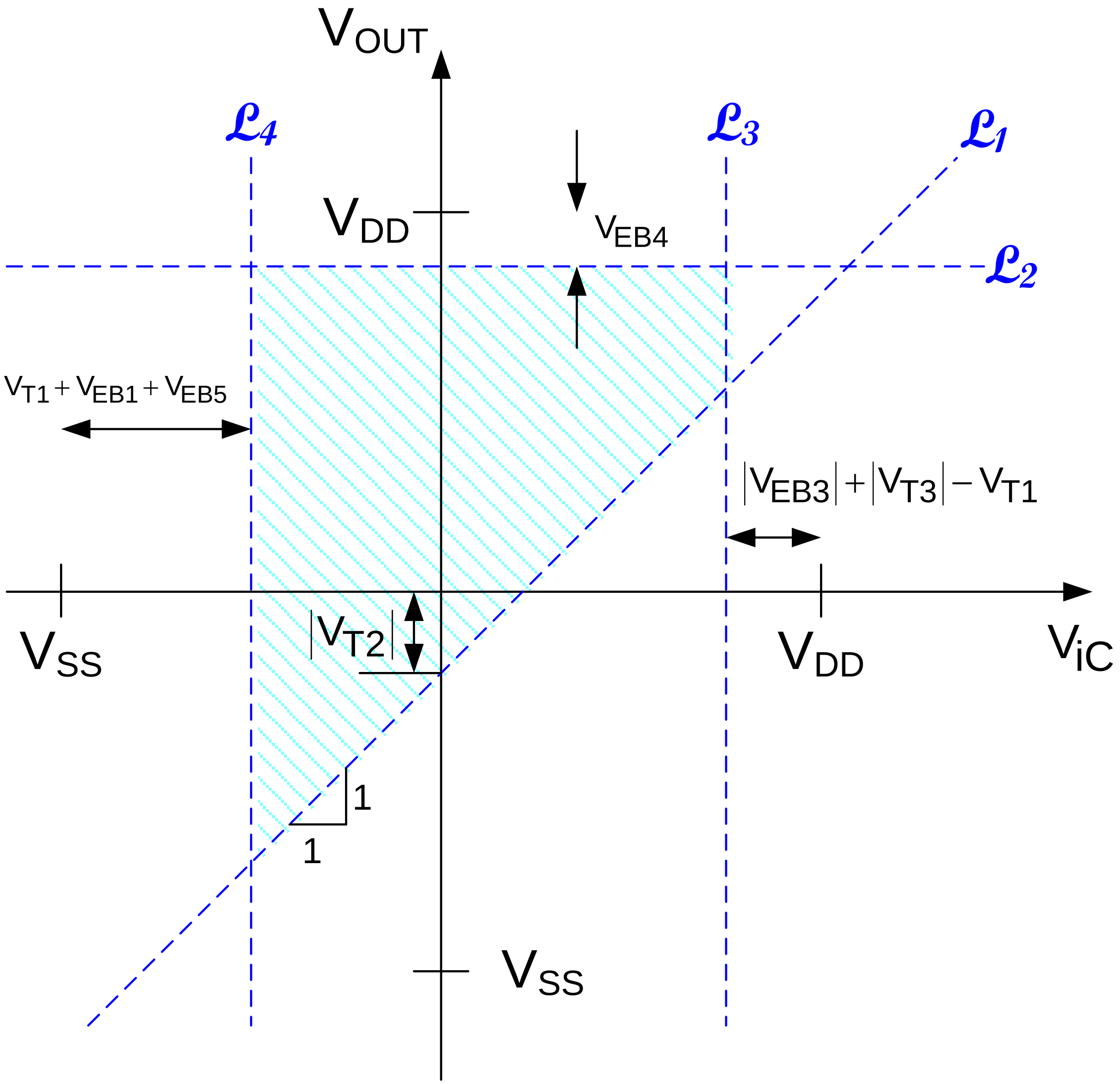
$\mathcal{L}_2$: $$V_{OUT} < V_{DD} - \left|V_{EB4}\right|$$

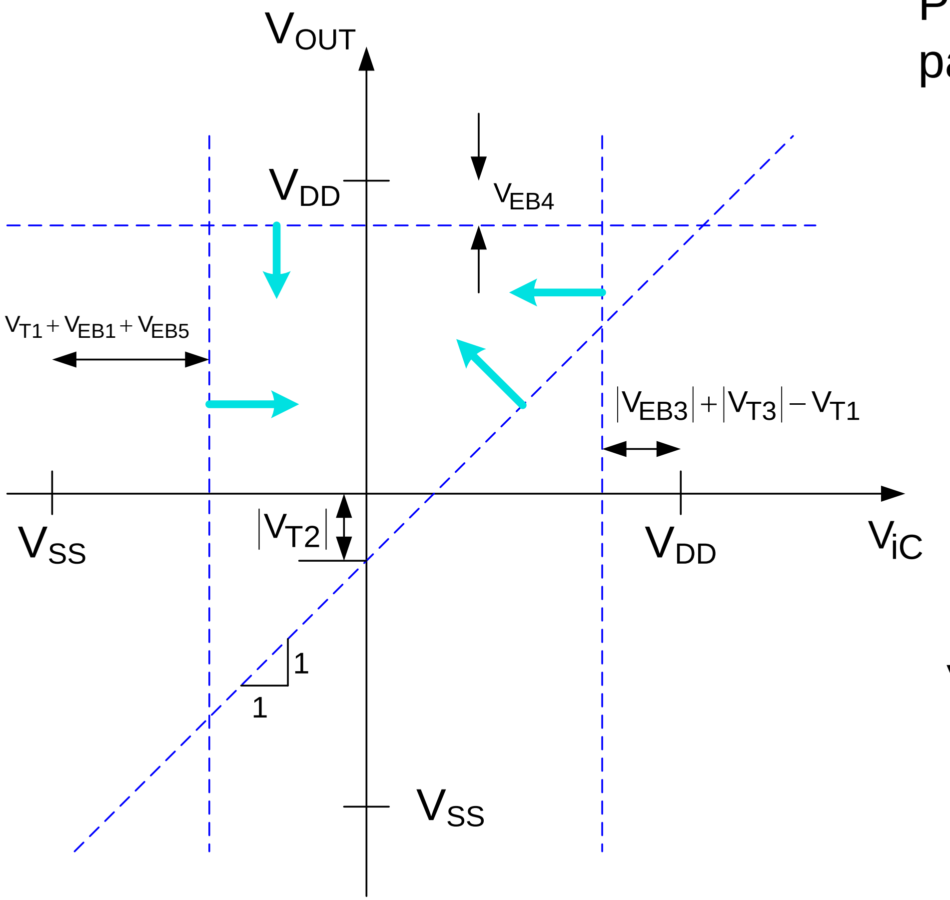
$\mathcal{L}_3$: $$V_{iC} < V_{DD} + V_{T1} - \left|V_{T3}\right| - \left|V_{EB3}\right|$$

$\mathcal{L}_4$: $$V_{ic} > V_{T1} + V_{EB1} + V_{EB5} + V_{SS}$$

Signal Swing of Single-Stage 5T Op Amp



Signal Swing of Single-Stage Op Amp



Preemptive comment: practical parameter domain for 5T Op Amp

$\{V_{EB1}\ V_{EB3}\ V_{EB5}\ \ P\}$

Constraining Equations:

$$V_{OUT} > V_{ic} - V_{T2}$$

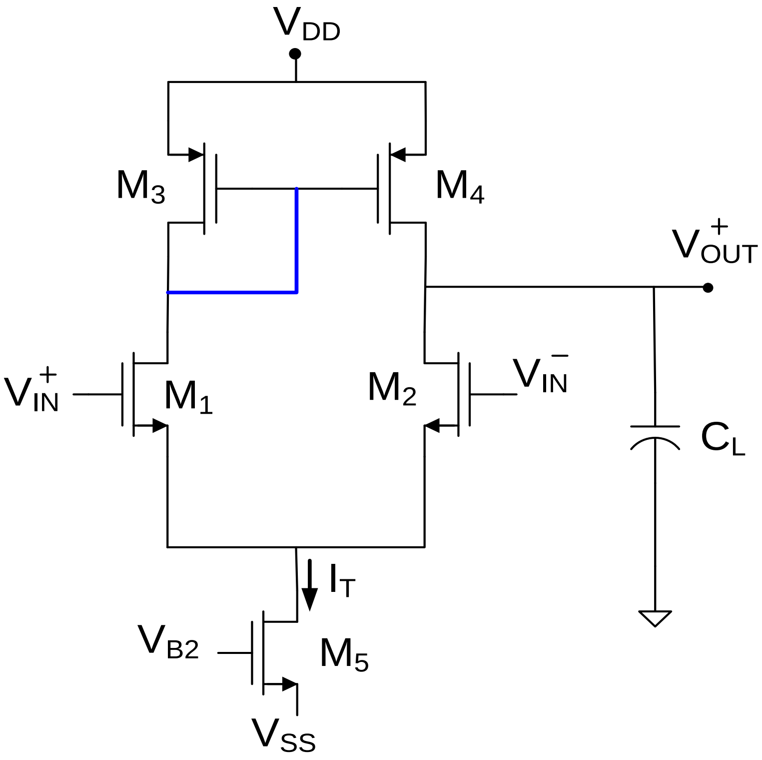
$$V_{OUT} < V_{DD} - |V_{EB4}|$$

$$V_{iC} < V_{DD} + V_{T1} - |V_{T3}| - |V_{EB3}|$$

$$V_{ic} > V_{T1} + V_{EB1} + V_{EB5} + V_{SS}$$

- Signal swings are Important Performance Parameters !!
- Signal swing parameters are naturally in practical parameter domain

Design space for single-stage 5T op amp



How many independent design variables and how many constraints does this circuit have (assuming symmetry)?

Assume V_{SS}, V_{DD}, and C_L fixed

Small-signal domain?

$\{g_{m1}, g_{m3}, g_{m5}, g_{01}, g_{03}, g_{05}\}$

(not independent)

Natural parameter domain?

$\{W_3/L_3, W_1/L_1, W_5/L_5, I_T\}$

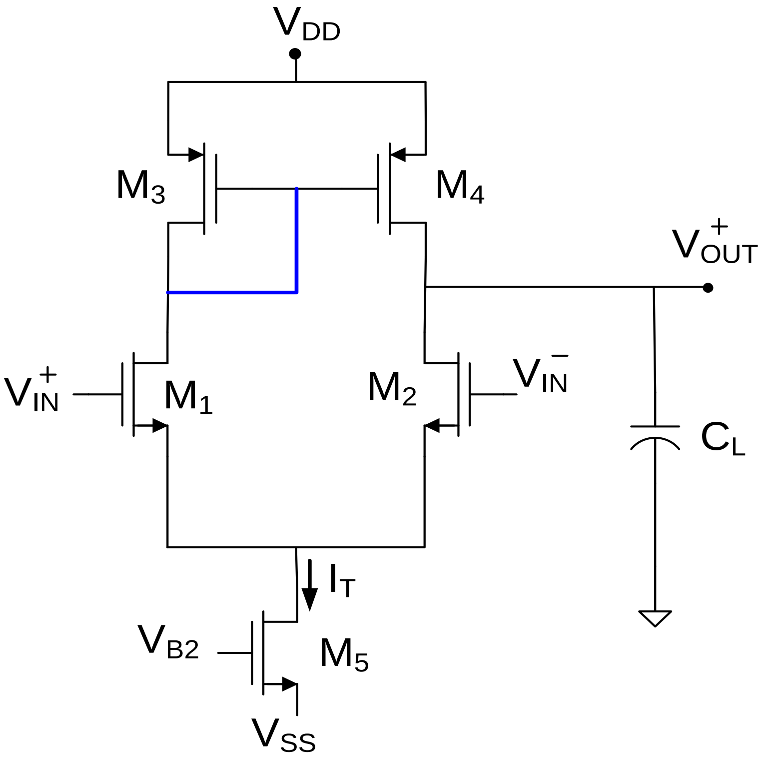
No constraints

A practical parameter domain?

$\{ V_{EB1}\ V_{EB3}\ V_{EB5}\ \ P\}$

No constraints

Design space for single-stage 5T op amp



Performance Parameters in Practical Parameter Domain $\{V_{EB1}\ V_{EB3}\ V_{EB5}\ P\}$:

$$A_0 = \left[\frac{1}{\lambda_1 + \lambda_3}\right]\left(\frac{2}{V_{EB1}}\right)$$

$$GB = \left(\frac{P}{V_{DD} C_L}\right)\left[\frac{1}{V_{EB1}}\right]$$

$$SR = \frac{P}{(V_{DD} - V_{SS}) C_L}$$

$$V_{OUT} < V_{DD} - |V_{EB3}|$$

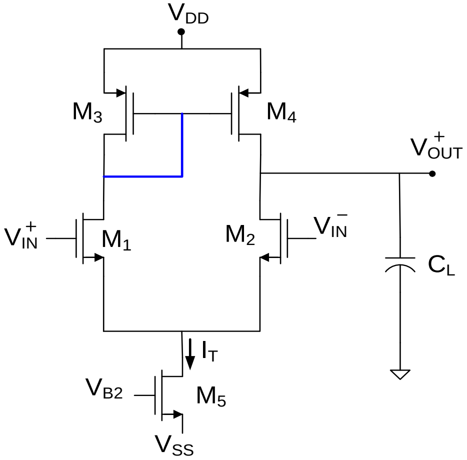
$$V_{OUT} > V_{ic} - V_{T2}$$

$$V_{iC} < V_{DD} + V_{T1} - |V_{T3}| - |V_{EB3}|$$

$$V_{ic} > V_{T1} + V_{EB1} + V_{EB5} + V_{SS}$$

Simple Expressions (7) in Practical Parameter Domain

Design example for single-stage 5T op amp



Performance Parameters in Practical Parameter Domain $\{ V_{EB1}\ V_{EB3}\ V_{EB5}\ \ P \}$:

$$A_0 = \left[\frac{1}{\lambda_1 + \lambda_3}\right]\left(\frac{2}{V_{EB1}}\right)$$

$$GB = \left(\frac{P}{V_{DD}C_L}\right)\left[\frac{1}{V_{EB1}}\right]$$

$$SR = \frac{P}{(V_{DD} - V_{SS})C_L}$$

$$V_{OUT} < V_{DD} - |V_{EB3}|$$

$$V_{OUT} > V_{ic} - V_{T2}$$

$$V_{iC} < V_{DD} + V_{T1} - |V_{T3}| - |V_{EB3}|$$

$$V_{ic} > V_{T1} + V_{EB1} + V_{EB5} + V_{SS}$$

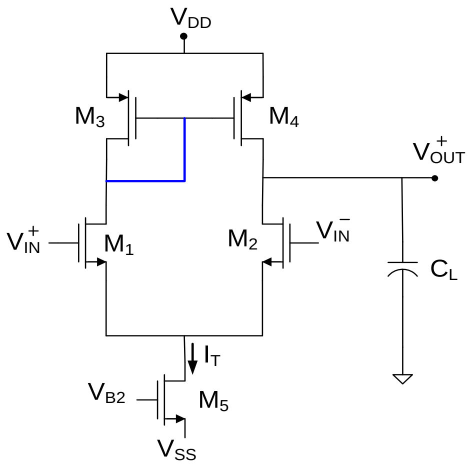
Assume design to meet A_0, GB and signal swing specs.

1. Select Parameter Domain (will use practical parameter domain) $\{ V_{EB1}\ V_{EB3}\ V_{EB5}\ \ P \}$
2. Pick V_{EB1} to meet gain requirement) $\{ \cancel{V_{EB1}}\ V_{EB3}\ V_{EB5}\ \ P \}$

$$V_{EB1} = \left[\frac{1}{\lambda_1 + \lambda_3}\right]\left(\frac{2}{A_0}\right)$$

3. Pick P to meet GB requirement $\{ \cancel{V_{EB1}}\ V_{EB3}\ V_{EB5}\ \cancel{P} \}$
4. Pick V_{EB3} and V_{EB5} to meet signal swing requirements
5. Map back from the Practical Parameter Domain to the Natural Parameter domain (next page)

Design example for single-stage 5T op amp



Performance Parameters in Practical Parameter Domain $\{V_{EB1}\ V_{EB3}\ V_{EB5}\ \ P\}$:

Mapping from Practical Parameter Domain $\{V_{EB1}\ V_{EB3}\ V_{EB5}\ \ P\}$ to Natural Parameter Domain $\{W_1/L_1\ \ W_3/L_3\ \ W_5/L_5\ \ I_T\}$

From expression $I_{Dk} = \dfrac{\mu_k C_{ox} W_k}{2L_k} V_{EBk}^2$ it follows that

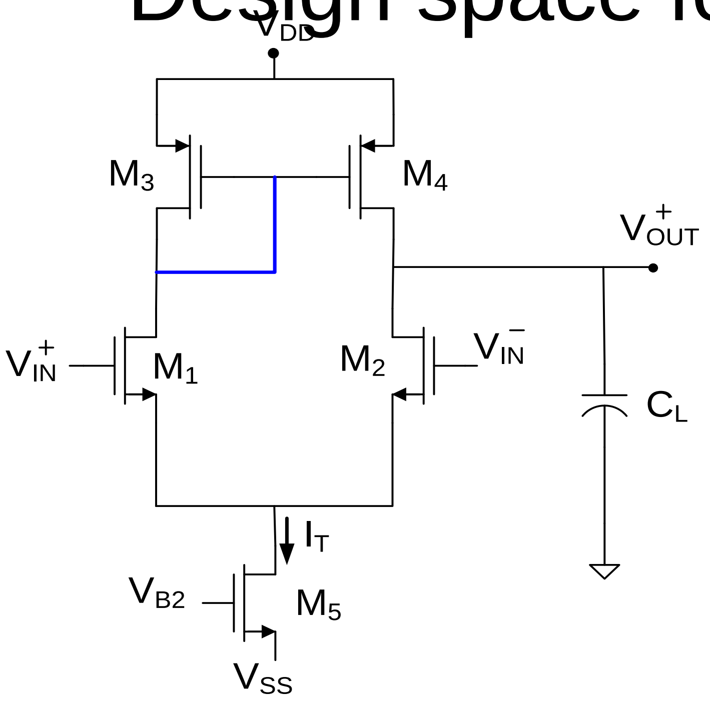
$$\frac{W_1}{L_1} = \frac{1}{\mu_n C_{OX} V_{EB1}^2} \frac{P}{V_{DD} - V_{SS}}$$

$$\frac{W_3}{L_3} = \frac{1}{\mu_p C_{OX} V_{EB3}^2} \frac{P}{V_{DD} - V_{SS}}$$

$$\frac{W_5}{L_5} = \frac{2}{\mu_n C_{OX} V_{EB5}^2} \frac{P}{V_{DD} - V_{SS}}$$

$$I_T = \frac{P}{V_{DD} - V_{SS}} \quad \text{or} \quad V_{B2} = V_{EB5} + V_{ss} + V_{THn}$$

Design space for single-stage 5T op amp



Performance Parameters in Natural Parameter Domain $\{ W_1/L_1 \;\; W_3/L_3 \;\; W_5/L_5 \;\; I_T \}$:

$$A_{V0} = \left[\frac{\sqrt{4\mu_n C_{OX}}}{\lambda_1 + \lambda_3} \right] \left(\frac{\sqrt{\frac{W_1}{L_1}}}{\sqrt{I_T}} \right)$$

$$SR = \frac{I_T}{C_L}$$

$$GB = \left[\frac{\sqrt{\mu_n C_{OX}}}{C_L} \right] \sqrt{\frac{W_1}{L_1}} \sqrt{I_T}$$

$$V_{iC} < V_{DD} + V_{T1} - \left| V_{T3} \right| - \frac{\sqrt{I_T}}{\sqrt{\mu_p C_{OX}} \sqrt{\frac{W_3}{L_3}}}$$

$$V_{OUT} < V_{DD} - \frac{\sqrt{I_T}}{\sqrt{\mu_p C_{OX}} \sqrt{\frac{W_3}{L_3}}}$$

$$V_{ic} > V_{T1} + \frac{\sqrt{I_T}}{\sqrt{\mu_n C_{OX}} \sqrt{\frac{W_1}{L_1}}} + \frac{\sqrt{I_T}}{\sqrt{\mu_n C_{OX}} \sqrt{\frac{W_5}{L_5}}} + V_{SS}$$

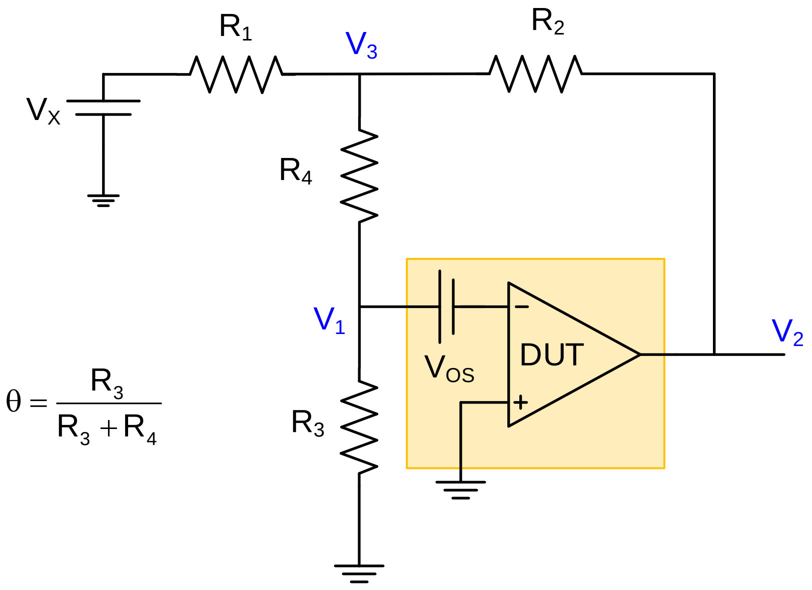
$$V_{OUT} > V_{ic} - V_{T2}$$

Complicated Expressions (7) in Practical Parameter Domain

Measurement and Simulation of Op Amps

- Measurement of A_V is challenging
  - Because it is so large
  - Even harder as A_{V0} becomes larger
  - Offset voltage causes a problem
  - Embed in Feedback Network to Stabilize Operating Point
    - Stability must be managed
    - Use time varying input to distinguish signal information from offset
    - Must be well below first pole frequency to measure A_{v0}
  - Measurement challenges often parallel simulation challenges
- Measurement of GB by indirect closed loop BW measurement is easy
- Measurement of R_0 is challenging
  - Often very small
  - Often challenging to avoid having measurement circuit cause output current to exceed I_{OMAX}

Measurement and Simulation of Op Amps



$$\theta = \frac{R_3}{R_3 + R_4}$$

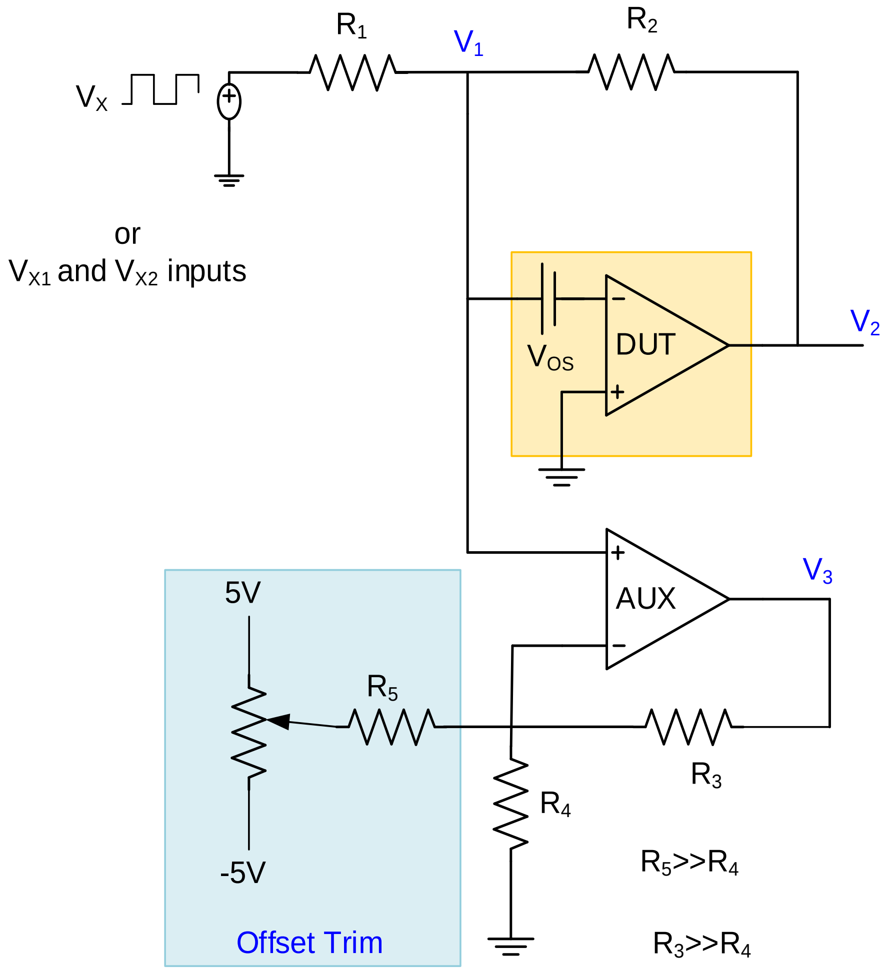
Consider two inputs, V_{X1} and V_{X2}

$$\left.\begin{aligned}
V_{21} &= -A\left(\theta V_{31} - V_{OS}\right) \\
V_{22} &= -A\left(\theta V_{32} - V_{OS}\right) \\
V_{31}\left(G_1 + G_2 + G_4\right) &= G_1 V_{X1} + G_2 V_{21} \\
V_{32}\left(G_1 + G_2 + G_4\right) &= G_1 V_{X2} + G_2 V_{22}
\end{aligned}\right\}$$

$$A = \frac{1}{\theta}\frac{V_{22} - V_{21}}{V_{31} - V_{32}}$$

$$V_{OS} = \theta\frac{V_{21}V_{32} - V_{31}V_{22}}{V_{21} - V_{22}}$$

Measurement and Simulation of Op Amps

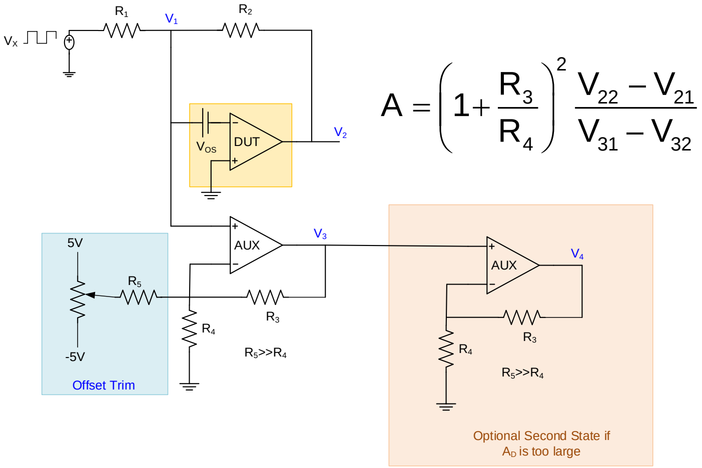


or
V_{X1} and V_{X2} inputs

Consider two inputs, V_{X1} and V_{X2}

$$A=\left(1+\frac{R_3}{R_4}\right)\frac{V_{22}-V_{21}}{V_{31}-V_{32}}$$

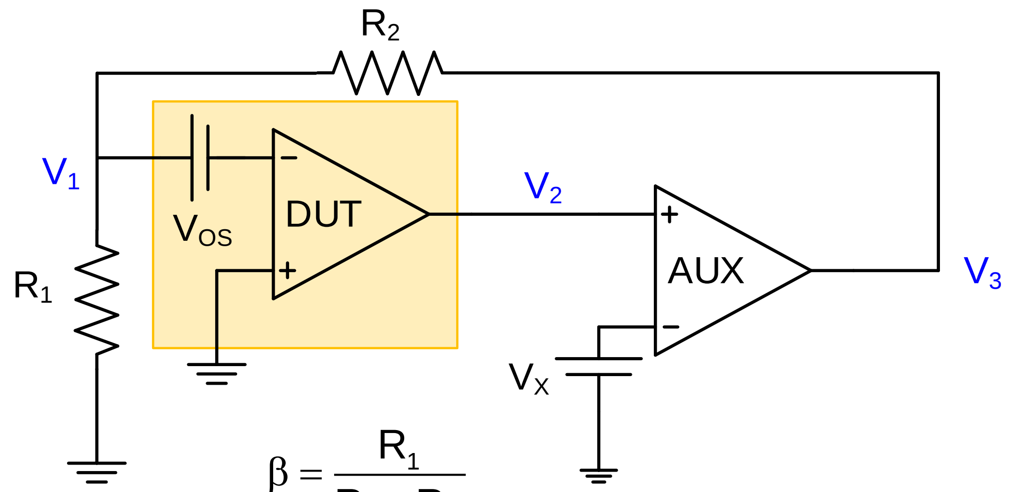
Can also measure V_{OS} with this circuit



$$A=\left(1+\frac{R_3}{R_4}\right)^2\frac{V_{22}-V_{21}}{V_{31}-V_{32}}$$

Can add gain stage if A is very large

Measurement and Simulation of Op Amps



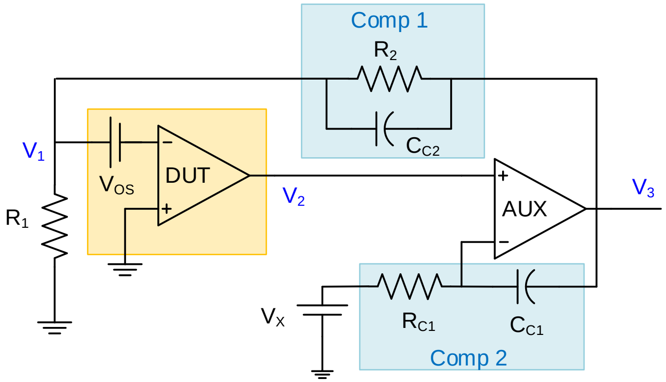
$$\beta = \frac{R_1}{R_1 + R_2}$$

Consider two inputs, V_{X1} and V_{X2}

$$V_{OS} = \frac{\beta\left(V_{32}\dfrac{V_{X1}}{V_{X2}} - V_{31}\right)}{\left(\dfrac{V_{X1}}{V_{X2}} - 1\right)}$$

$$A_V = \frac{V_{X2} - V_{X1}}{\beta\left(V_{31} - V_{32}\right)}$$

- Must compensate this circuit and compensation may be a bit complicated
- Compensation beyond scope at this stage in EE 435



Potential Compensation Structures

Laboratory Support

Problems observed in laboratory

- Could not see gain (signals were too small)
  - Did not know how big of signals to expect
  - Amplifier offset made it difficult to see output
  - Output was real noisy
    - (be sure to use V_{DD} and V_{SS} bypass capacitors)
- Gain did not agree with expected results
  - Not operating at right Q-point
  - Amplifier was defective
  - Multimeter used incorrectly to measure gain
  - (Always use scope to monitor signals!)
- Buffer amplifier did not have right gain
  - Voltage on protoboard pin did not agree with voltage on op amp pin
- Sparks fly when connected scope to circuit
  - Red and black banana jack barrels on terminator were switched

Laboratory Support

Problems observed in laboratory

- Signal generator was defective because monstrous noise on output
  - Scope was not appropriately triggered
- Did not see output waveform from signal generator
  - Horizontal time base setting was orders of magnitude off
  - Vertical amplifier setting was orders of magnitude off
  - **Auto-find function on scope is not your friend !!!!!**
- Signals on scope were too noisy
  - Bandwidth limit on scope useful for eliminating high frequency noise from measurement environment

Laboratory Support

Problems observed in laboratory

- Ground and common were somewhat randomly interconnected

Earth ground corresponds to the third prong on a standard 120 V connector and is connected to a large conducting rod that is driven deeply into the surface of the earth somewhere in our around the building. The chasis (if metal) on test equipment is usually connected to the third prong on the power supply cable and the metal on the benches is usually connected independently to earth ground.

The ground (black) conductor on most test equipment and the outside conductor on BNC connectors is usually connected to the third prong on the power supply cable and thus to earth ground.

Circuit ground is whatever you decide to call it but designers usually connect it to earth ground.

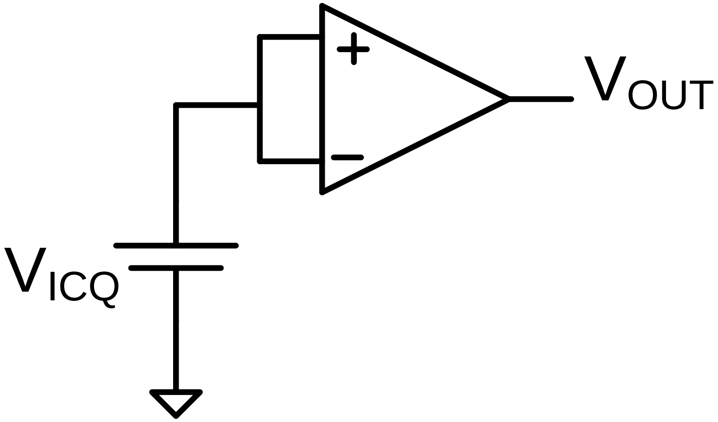
Common on dc power supplies is usually floating at low frequencies relative to earth ground as are the positive and negative terminals of the dc power supplies.

Everything connected to earth ground is connected together and no ac or dc signal source can be connected "between" two earth ground connections !!

Laboratory Support

Offset Voltage

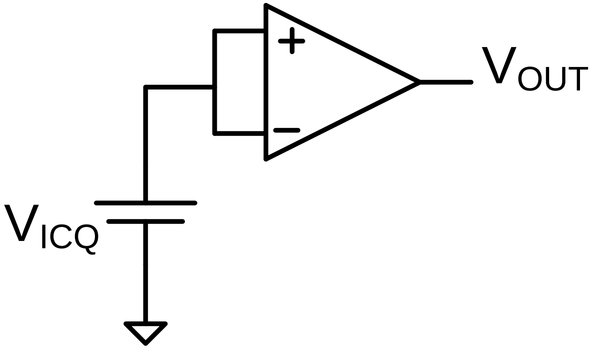
- Systematic Offset Voltage
- Random Offset Voltage



Laboratory Support

Offset Voltage

- Systematic Offset Voltage
- Random Offset Voltage

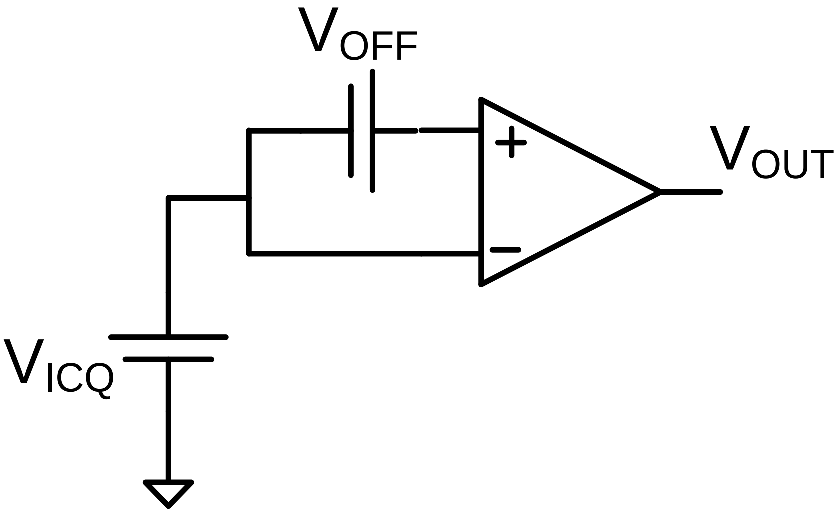


Definition: The output offset voltage is the difference between the desired output and the actual output when V_{id}=0 and V_{ic} is the quiescent common-mode input voltage.

$$V_{OUTOFF} = V_{OUT} - V_{OUTDES}$$

Note: V_{OUTOFF} is dependent upon V_{ICQ} although this dependence is usually quite weak and often not specified

Laboratory Support



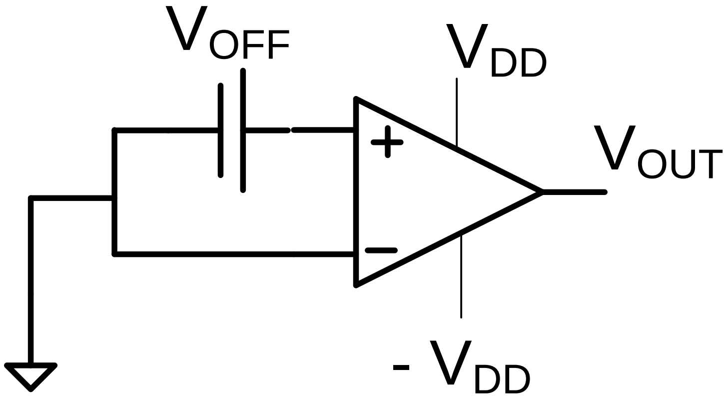
Definition: The input-referred offset voltage is the differential dc input voltage that must be applied to obtain the desired output when V_{ic} is the quiescent common-mode input voltage.

Note: V_{OFF} is usually related to the output offset voltage by the expression

$$V_{OFF} = \frac{V_{OUTOFF}}{A_D}$$

Note: V_{OFF} is dependent upon V_{ICQ} although this dependence is usually quite weak and often not specified

Laboratory Support

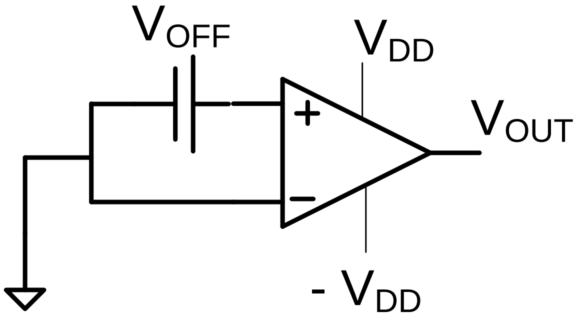


When differential input op amps are biased with symmetric supply voltages, it is generally assumed that the desired quiescent input voltage Is 0V and the desired quiescent output voltage is 0V so V_{OFF} is the differential Input voltage needed to make V_{OUT}=0V.

The input offset voltage is comprised of two parts, a systematic component and a random component

$$V_{OFF} = V_{OFFSYS} + V_{OSR}$$

Laboratory Support



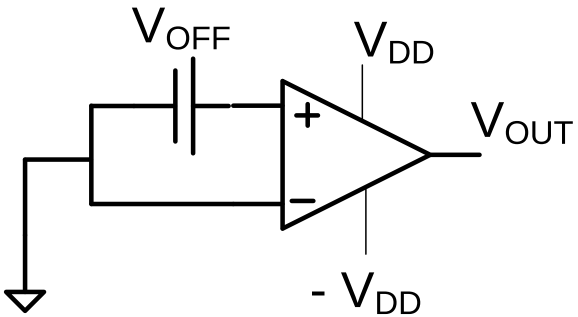
$$V_{OFF} = V_{OFFSYS} + V_{OSR}$$

After fabrication there is no distinction made between V_{OFFSYS} and V_{OSR} and simply V_{OFF} is of concern

V_{OSR} is determined entirely by random variations in component values from Their ideal value and will only be seen in a simulation if deviations are intentionally introduced (Monte Carlo Analysis if often used for predicting V_{OSR})

It is expected that V_{OFFSYS} should be small (much smaller than V_{OSR}) and it is the designer's responsibility to make this small

Laboratory Support

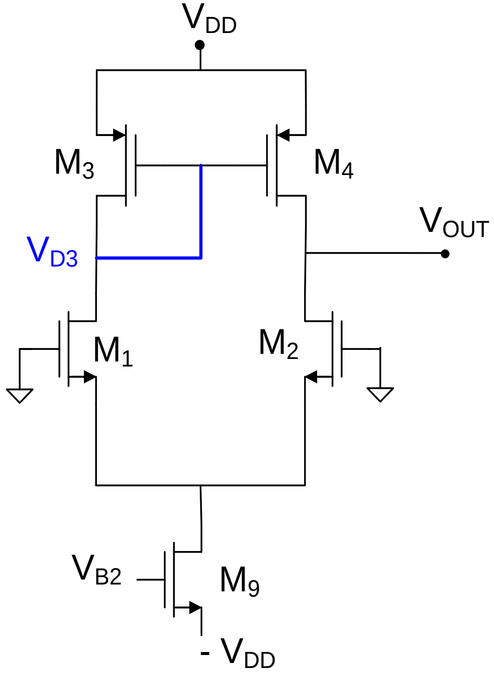


$$V_{OFF} = V_{OFFSYS} + V_{OSR}$$

It is not necessary to make V_{OFFSYS} =0 although this can and is often done by making a minor tweak of matching critical parameters after the design of the op amp is almost complete

V_{OFFSYS} can also be set to 0 by using a degree of freedom of the amplifier design variables but this is generally an unwise use of degrees of freedom (although some textbooks including Martin and Johns in Sec 5.1 do this!)

Laboratory Support

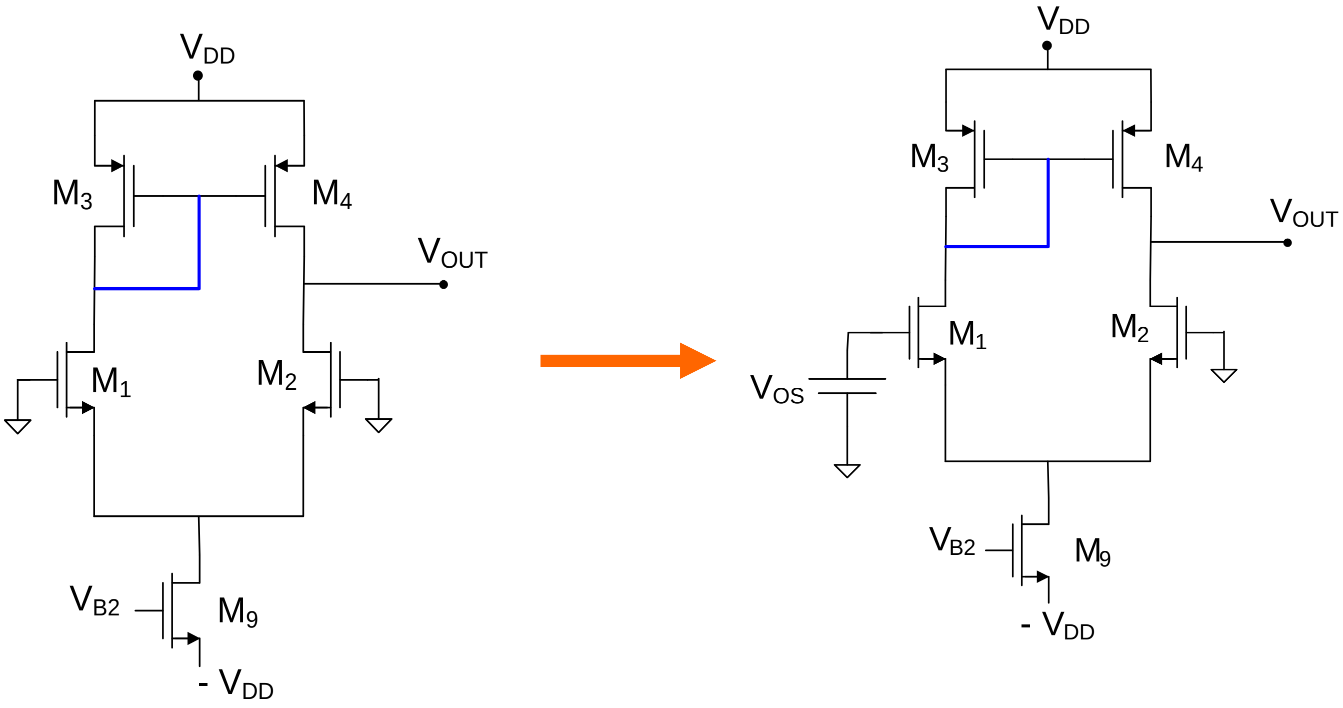


(If no missmatch is introduced, will be seeing only effects of systematic offset)

By symmetry, to force $V_{OUT} = 0$, it is necessary to have $V_{D3}=0$

- Making $V_{D3}=0$ sets $|V_{EB3}| = V_{DD} + V_{Tp}$ and results in the use of one degree of freedom!
- Making V_{EB3} so large will severely limit the voltage swing at V_{OUT}
- This shows why it is not wise to use a degree of freedom to make desired output voltage 0

Laboratory Support

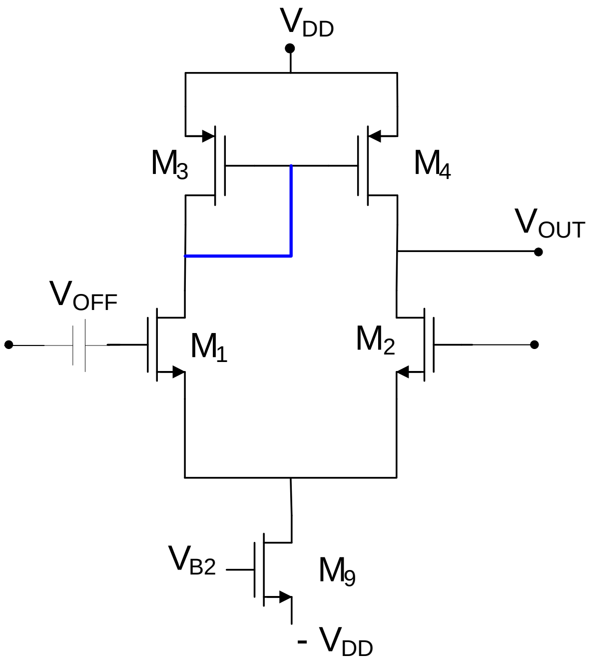


Can sweep a voltage in simulator at gate of M_1 to make $V_{OUT}=V_{OUT\_DESIRED}$

This is the systematic offset voltage

Can simply add the systematic offset voltage to input throughout rest of the design phase and then remove after design is complete or tweak at end of design to eliminate systematic offset.

Laboratory Support



Usually V_{OFF} will change if changes in any design variables are made so re-simulation will be needed to get the correct value of V_{OFF}

If V_{OFF} is not included, ac simulation of open-loop amplifier will usually not give desired results because small-signal models will be developed in simulator at incorrect operating point (often even in incorrect region of operation)

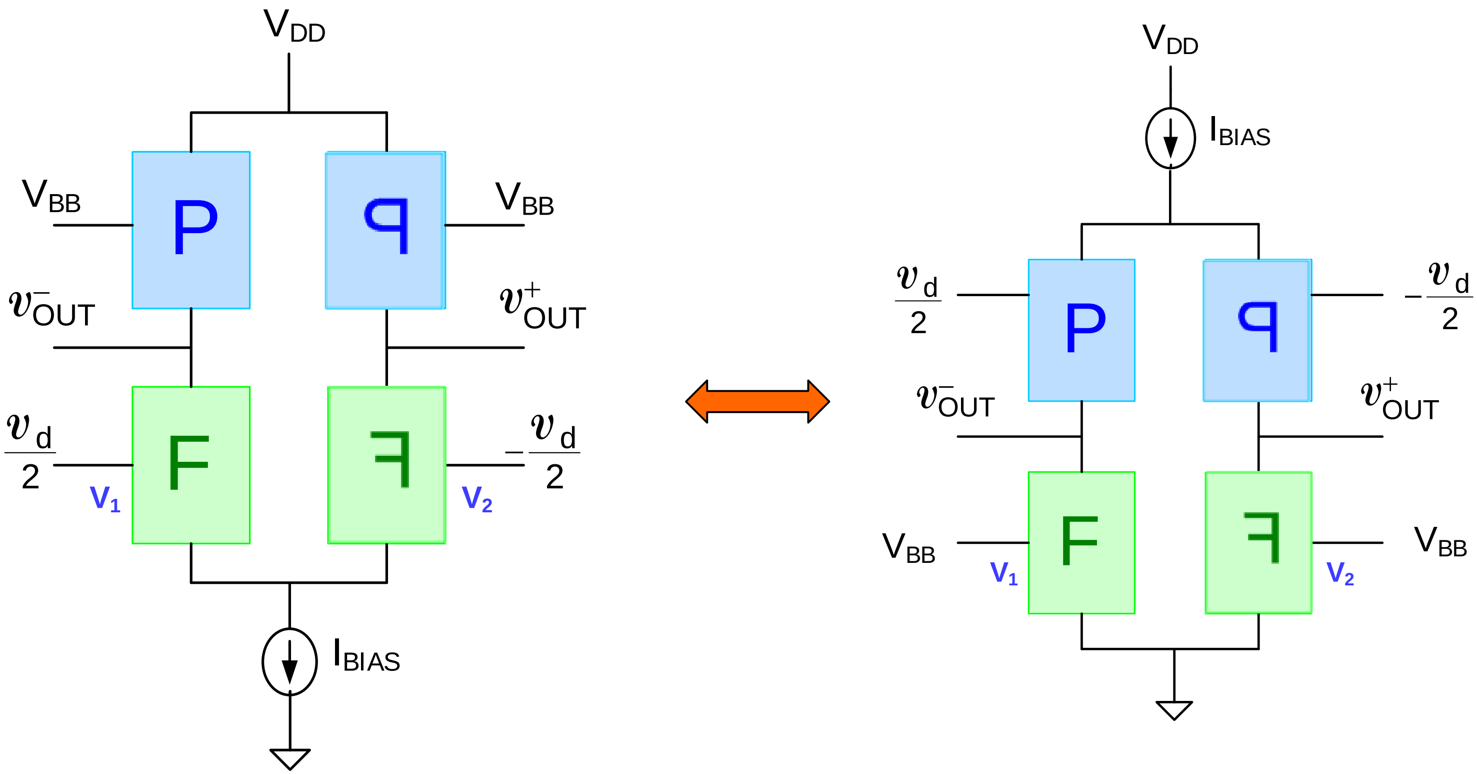
Alternative is to do ac simulations by embedding op amp into a FB configuration that will inherently compensate for offset voltage but issue of compensation must be addressed for amplifiers with two or more poles

Where we are at:

Basic Op Amp Design

- Fundamental Amplifier Design Issues
- Single-Stage Low Gain Op Amps
- Single-Stage High Gain Op Amps
- Other Basic Gain Enhancement Approaches
- Two-Stage Op Amp

Inputs into Counterpart Circuit or Quarter Circuit



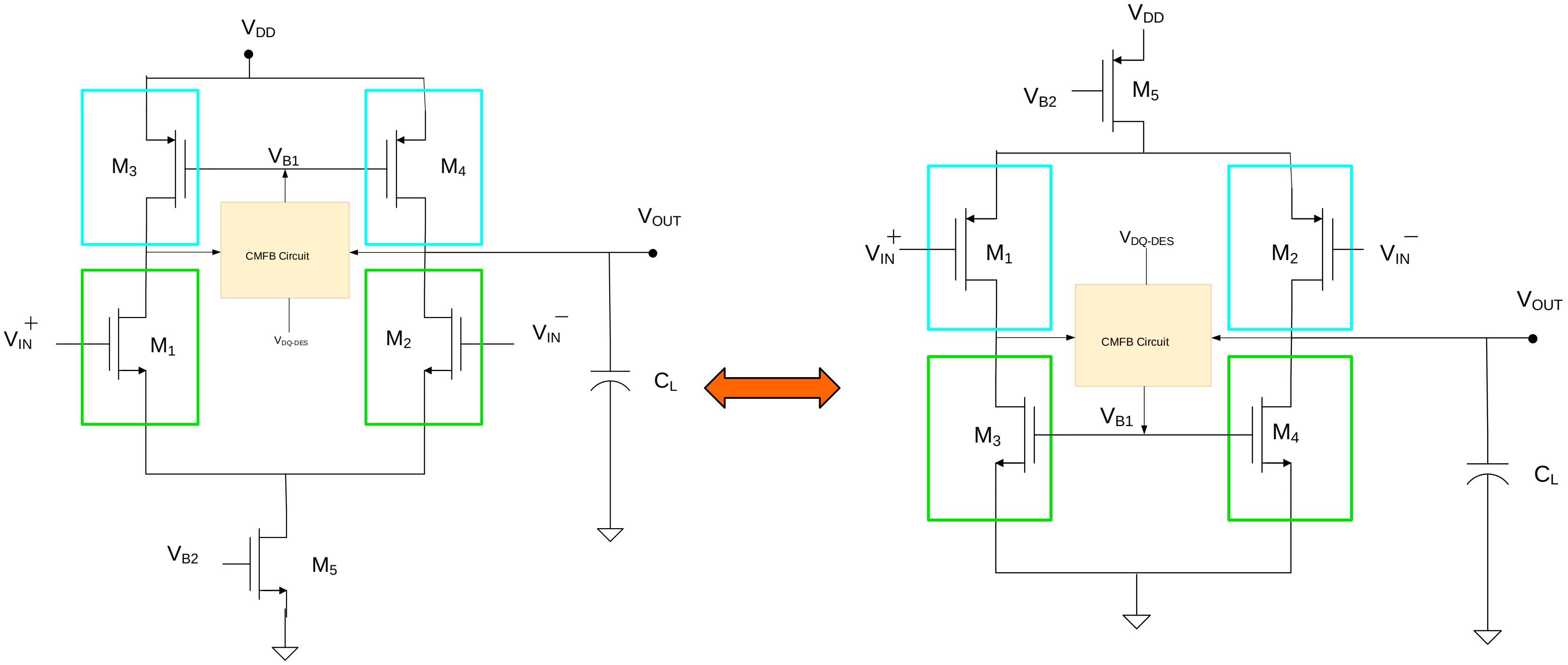
Gain, BW, and GB expressions identical

- This is a general concept not related to what type of quarter circuit is used
- Performance may be different because n-channel and p-channel performance different

Inputs into Counterpart Circuit or Quarter Circuit for single-transistor quarter circuit

5T Op Amp with n-ch inputs

5T Op Amp with p-ch inputs



Gain, BW, and GB expressions identical

- Performance may be different because n-channel and p-channel performance different
- Both are widely used

Single-stage op amps

Question – is the gain achievable with the single-stage low-gain op amps using a single MOS transistor as a quarter circuit adequate?

$$\mathbf{A_{V0}} = \left[\frac{\mathbf{1}}{\boldsymbol{\lambda_1} + \boldsymbol{\lambda_3}}\right]\left(\frac{\mathbf{1}}{\mathbf{V_{EB1}}}\right)$$

If $\lambda_1=\lambda_3=.01V^{-1}$ and $V_{EB1}=.15V$, then

$$A_{V0} \approx \frac{1}{(.01+.01)}\frac{1}{0.15} = 333$$

or, in db, $A_{V0db}=20\log_{10}333=50db$

This is inadequate for many applications !

What can be done about it ?

Stay Safe and Stay Healthy !

End of Lecture 6